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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,911	11/21/2003	Shui-Ming Cheng	TSM03-0694	2406

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EXAMINER	
LINDSAY JR, WALTER LEE	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,911	CHENG, SHUI-MING	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- Th MAILING DATE of this communication app ars on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 11-20* is/are pending in the application.

4a) Of the above claim(s) *6-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,11-14 and 16-20* is/are rejected.

7)☒ Claim(s) *5 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/21/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the Election requirement filed 6/3/2004.

Currently, claims 1-5 and 11-20 are pending. Claims 6-10 have been withdrawn.

Election/Restrictions

1. Claims 6-10 have withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 6/3/2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-4, 11-14 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (U.S. Patent No. 5,908,313 patented 6/1/1999) in view of Skotnicki et al. (U.S. Patent No. 6,724,660 filed 12/12/2001).

Chau shows the method substantially as claimed, in Figs 3a-3e and corresponding text as: forming a recess (312) in a substrate (300) adjacent a gate (306) of said transistor(col. 5, lines 23-44); forming a deep-doped region (313) below a bottom surface of said recess (col. 6, lines 42-54)(claim 1). Forming a lightly doped drain region (308) adjacent said gate (col. 5, line 57-col. 6, line 5)(claim 2). Chau describes the method, wherein said semiconductor material is silicon (col. 4, lines 56-67)(claim 3). Chau describes the method, wherein said forming said deep doped region is performed by an ion implantation process (col. 6 lines 42-54)(claim 4). Chau also substantially shows: providing a gate on a substrate, including: forming a gate dielectric (302) over said substrate and forming a gate electrode (306) over said gate dielectric (col. 5, lines 23-44); and providing a source/drain, including: forming a recess in said substrate adjacent said gate, forming a deep doped region below a bottom surface of said recess (col. 6, lines 42-54) (claim 11). Forming a lightly doped drain region (308) adjacent said gate (col. 5, lines 57-5)(claim 12). Wherein said semiconductor material is silicon (col. 4, lines 56-67)(claim 13). Chau describes the method, wherein said forming said deep doped region is performed by an ion implantation process (col. 6 lines 42-54)(claim 14). Chau inherently teaches: forming another recess in said substrate adjacent said gate(col. 6, lines 42-54); forming a deep-doped region below a bottom surface of said another recess(col. 6, lines 42-54) (claim 16). Chau describes the method, wherein said providing said another source/drain further includes forming a lightly doped drain region adjacent said gate (col. 5, line 57-col. 6 line 5)(claim 17). Chau describes the method, wherein said semiconductor material is silicon (col. 4, lines 56-67)(claim 18).

Chau describes the method, wherein said providing said gate further includes forming spacers (310) on opposing walls of said gate dielectric (302) and gate electrodes (302) (col. 9, lines 38-63) (claim 19). Chau describes the method, wherein said providing said gate and said source/drain further include performing a silicide process to form contacts thereon (col. 9, lines 38-63) (claim 20).

Chau lacks anticipation only in not explicitly teaching that: epitaxially growing a semiconductor material within said recess to form said source/drain (claims 1, 11 and 16).

Skotnicki teaches a method of forming recesses in a semiconductor substrate in a similar semiconductor device. In fig. 4f shows selective epitaxial growth silicon that fills recesses 25 and 26. This region is then doped to form a source/drain region (col. 6, lines 24-27).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method shown in Chau by using the selective epitaxial growth silicon as formed in Skotnicki, with the motivation that both Chau and Skotnicki look to reduce junction capacitance without surrendering read sensitivity.

Allowable Subject Matter

5. Claims 5 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...wherein said ion implantation process comprises implanting one of P-type ions and N-type ions, as required by claims 5 and 15.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WLL
June 24, 2004

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800